ASYMMETRIC COMPENSATION CIRCUIT

BACKGROUND OF THE INVENTION

1. Field of the Invention

[01]   This invention relates in general to the field of information storage, and more particularly to correcting an asymmetric signal resulting from the use of magneto-resistive (MR) transducing heads in hard disk drives (HDD), and more particularly in HDD read channels.

2. Description of the Related Art

[02]   Fig. 10 shows a schematic representation of a typical HDD, including at least one disk 1006 having a magnetic medium for storing information, a spindle, a motor 1007, and a controller 1008 for controlling disk rotational speed, a transducing head 1005 (for reading and writing data), a servo actuator assembly including a positioning controller for positioning the head over the appropriate disk track 1004, and data channels 1003 for transmitting data to and from the disk. The transducing head 1005 reads data from and writes data to the disk in data blocks having either fixed or variable length. A data block comprises a preamble (for acquiring timing signals), timing bits, a position error field, address bits, data bits, and error correction bits. Data blocks are recorded in sectors in concentric tracks. A track may comprise several sectors. The number of sectors may depend on the radial location of the track on the disk.

[03]   Data channels on an HDD transmit and receive data via a communication medium. HDD and communication systems can utilize similar techniques to encode data for storage and retrieval or for transmission and reception wherein data is encoded into a form in which it may be easily manipulated. Most modern applications of such systems encode data as numeric or digital information, wherein discrete numeric values are used to represent user data.

[04]   The storage or communication media do not directly manipulate such digital data. Rather, these media store or transmit analog signals representative of the digital data. For example, encoded digital information may be represented as magnetic flux changes stored in the magnetic media of a hard drive. The data embodied in the medium are then received or

retrieved to decode the signals and reproduce the encoded digital data. A read channel is a circuit that reads or receives the encoded data and reproduces the original digital signal. In general, a read channel includes a transducer component that senses the analog signal and digital processing components that detect sequences of changes in the signal that represent encoded digital data. For example, a read channel used in a magnetic storage device includes a transducer head that senses the magnetic flux changes and produces a continuous analog signal that must then be detected and decoded. In general, certain peaks in the continuous waveform represent the encoded digital data.

[05]   Transducing heads may be either inductive or magneto-resistive (MR). An MR head is a device whose resistance varies with the applied magnetic field. In this regard, the head is capable of converting magnetic field variations produced by data into a time varying voltage or current in an electrical circuit. MR heads offer many advantages over other types of magnetic transducers and, consequently, are increasingly being used in HDDs. For example, MR heads are more sensitive than other types of read heads, such as thin film heads, and produce a stronger read signal. Also, MR heads have a better frequency response than other types of heads which use inductive coils as a sensing means. In addition, the read signal produced by an MR head is relatively insensitive to the relative velocity between the head and the medium, than is the case with other types of heads, because it is the level of the applied magnetic field which is sensed by an MR head and not the rate of change of magnetic flux lines through a coil. This is an advantage in systems where head/medium velocity may vary over a significant range. Lastly, because MR heads are not capable of writing data on a magnetic medium, magnetic data storage systems using MR read heads must include a separate write head thereby making it possible to optimize the read head and the write head for their particular functions.

[06]   A disadvantage of an MR read head is that it produces a signal with an asymmetric amplitude. For example, the asymmetric nature of the MR head may cause the signal produced by the read head reading data to be different than the magnetic signal applied to the write head for writing data. To overcome this problem, a bias current may be applied to the head to move the quiescent operating point of the head to be more asymmetric of the resistance characteristic. However, due to variation in the microstructure and magnetic

properties of the recording medium and other manufacturing variables, biasing cannot completely remove the asymmetric aspect of the signal.

[07]   One approach is to use a filter having varying tap weights to change the shape of the waveform. Another variation is having a digital filter differentiate the waveform into sample and recreate an equalized waveform. Both these approaches are relatively complex.

[08]   Another approach provides circuitry to detect the polarity of an asymmetric signal and to add or subtract a shift voltage to adjust for the asymmetry.

[09]   A disadvantage of these approaches is that the corrective circuitry is dependent upon layout and process parameters that are difficult to control. Therefore, a need exists to address the asymmetric signal effects produced by such MR heads by providing circuitry to overcome the problems and limitations of the prior art.

SUMMARY OF THE INVENTION

[10]   To address the stated need and fulfill other desired objectives, in accordance with the invention, a communications read channel provides circuitry for correcting an asymmetric signal from an MR head thereby reducing errors in read channels. The circuitry comprises a differential amplifier portion and a high speed switching portion for converting an asymmetric signal having a positive and a negative polarity into a signal having only a positive polarity.

BRIEF DESCRIPTION OF THE DRAWINGS

[11]   Figure 1 shows an asymmetric signal from an MR read head.

[12]   Figure 2 shows a gain transfer function for an amplifier to correct an asymmetric signal.

[13]   Figure 3 shows a block diagram of a portion of a read channel circuit having asymmetric correction.

[14]   Figure 4 shows a block diagram of circuitry currently used for implementing asymmetric correction.

[15]   Figure 5 shows signals and waveforms associated with the block diagram of Fig. 4.

[16]   Figure 6 shows a block diagram of one embodiment of the inventive circuitry.

[17]   Figure 7 shows a typical differential amplifier used in the inventive circuitry.

[18]   Figure 8 shows detailed circuitry of the g_m switch used in the inventive circuitry.

[19]   Figure 9 shows signals and waveforms associated with the inventive circuitry of Fig. 6.

[20]   Figure 10 shows a schematic representation of an HDD system.

DETAILED DESCRIPTION OF EMBODIMENTS

[21]   In a read channel having an MR head, the MR head provides a differential input signal having a positive signal, Vip, and a negative signal, Vin, with the maximum values of each being different thereby defining the asymmetric distortion of the signal. The time varying input signal is shown in Fig. 1. In order to remove the asymmetry, the signal passes through an amplifier having a gain for the negative portion of the signal that is different than the gain for the positive portion of the signal. Such an amplifier may have a gain transfer function as shown in Fig. 2. An amplifier having a differential gain removes the asymmetric distortion from the signal.

[22]   A block diagram of a circuit for reducing the asymmetry is shown in Fig. 3. A variable gain amplifier (VGA) 310, receives the input signal, Vip-Vin, through a loading circuit 305, and provides the input to an asymmetry correction circuit (ASC) 320. The ASC 320 is an amplifier having a gain for the negative portion of the signal different from the gain for the positive portion of the signal, thereby removing the asymmetric distortion. The corrected signal passes in turn to an analog filter (AF) 330, an analog-to-digital converter buffer 340, and to the analog-to-digital converter (ADC) 350. The signal from the MR head is now corrected for asymmetric distortion.

[23]   Fig. 4 shows a present implementation of asymmetry correction circuitry. A first variable gain amplifier 410 receives an asymmetric signal from an MR head, and provides an output to a second variable gain amplifier 420. While the drawing shows two VGAs, the system can use a single, two-stage VGA, potentially providing a larger range. The second amplifier 420 provides the signal to a squaring device 430 and to a delay circuit 440. The squaring device 430 provides an output that is proportional to a gain g times the square of the input and has only a positive polarity. The delay circuit 440 accounts for the delay in squaring the signal. The outputs of each of the squaring device 430 and the delay circuit 440

drive output amplifiers whose outputs are summed. Each of amplifiers 410, 420, and the respective output amplifiers 450, 460 are differential amplifiers as shown in Fig. 7. The output amplifiers are necessary to ensure that the asymmetry correction circuitry is process independent.

[24]   Fig. 5 identifies the signals associated with a present implementation for correcting an asymmetric signal. The asymmetric signal is (Vip-Vin), and the square of this signal times a gain g, $g * (Vip-Vin)^2$, combines with the original signal to produce an output signal having a gain for the positive portion of the asymmetric signal different than the gain for the negative portion. The amount of positive and negative gain may be adjusted by varying the gain g of the squaring device 430.

[25]   In contrast, Fig. 6 shows the inventive circuit for the asymmetry correction circuitry, wherein a first variable gain amplifier 610 drives a second variable gain amplifier 620 and a g_m switch 630 coupled in parallel to amplifier 620. Each of amplifiers 610 and 620 may be circuits as shown in Fig. 7. The g_m switch 630 comprises a differential amplifier coupled with high speed switches as shown in Fig 8. The output of the g_m switch 630 combines with the output of amplifier 620 thereby providing a signal having corrected asymmetry.

[26]   Referring now to Fig. 8, the g_m switch 630 receives the differential input signals Vip and Vin and uses the input signals to generate a current proportional to the difference of Vip-Vin. The input signals also control the switching functions of the g_m switch.

[27]   The switching section further comprises two pair of high speed field effect transistors 810 (including transistors 812, 814) and 820 (including transistors 822, 824) for switching biasing current to the amplifier section. Each of the transistors 812, 814, 822, 824 is configured to have a sufficiently small linear range as measured by V_{dsat} (the voltage required to keep the transistors in saturation) that the transistors can behave as a switch. These characteristics of the transistors 812, 814, 822, 824 cause biasing current to flow through only the transistors having a positive gate, and not through the transistors having a negative gate. Therefore, whichever transistors are conducting are passing all the current. The current is not shared by each of the transistors of the switching pair. Ordinarily skilled artisans will be familiar with these characteristics, and the requisite linear range.

[28]   The source of transistor 812 connects to a first current source 860, the source of transistor 814 connects to a second current source 870, and the drains of transistors 812 and 814 are connected together and further connected to the source of transistor 832, one of the transistors of the amplifier section. Similarly, the source of transistor 822 is also connected to the first current source 860, and the source of transistor 824 is connected to the second current source 870. The drains of transistors 822 and 824 are also connected together and further connected to the source of transistor 834 of the amplifier section. The gates of transistors 812 and 824 are connected to the Vip input signal, and the gates of transistors 814 and 822 are connected together and further connected to the Vin input signal. Biasing resistors 840 and 850 are connected between current sources 860 and 870, and voltage is supplied by a common mode voltage source, Vcom. Biasing resistors 840 and 850 typically have the same value, but they may also have different values.

[29]   The amplifier section 830 is a differential amplifier comprising a pair of field effect transistors 832, 834. The source of transistor 832 is connected to the drain of the first pair of switching transistors 810, and the source of transistor 834 is connected to the drain of the second pair of switching transistors 820. The drains of transistors 832 and 834 are connected together and further connected to a third current source 880. The gate of transistor 832 is connected to Vip and the gate of transistor 834 is connected to Vin.

[30]   The differential amplifier is responsive to the differential input signal, Vip and Vin, producing a differential current, δi, proportional to the transconductance (or gain g_m) of the transistor pair 830 times the differential signal input voltage Vip-Vin. Therefore, a positive differential current δi flows through transistor 832 and correspondingly, a negative differential current, $-\delta i$, flows through transistor 834 when Vip is positive and Vin is negative. Conversely, when Vip is negative and Vip is positive, $-\delta i$ flows in transistor 832 and δi flows in transistor 834. Also, when Vip is positive, transistors 812 and 824 are conducting causing a current of 2 x δi to flow across the biasing resistors 840 and 850. When Vin is positive, transistors 814 and 822 are conducting, also causing a current of 2 x δi to flow across resistors 840 and 850. However, because of the high speed switching transistors reverse the current flow, the current flowing when Vin is positive flows in the same direction as when Vip is positive. Therefore, the current flows through resistors 840 and 850 in the

same direction irrespective whether the inputs are positive or negative. The output signal, taken across the biasing resistors 840 and 850, is proportional to the current, which is proportional to the differential input signal Vip-Vin.

[31]   Fig. 9 shows the different signals of the circuitry shown in Fig. 6. The asymmetric input signal to amplifier 620 and the g_m switch is Vip-Vin. The g_m switch provides a signal that is proportional to Vip-Vin but having only a positive polarity. The sum of these two signals shows the asymmetric correction circuitry having a different gain for the positive portion of the signal than for the negative portion of the signal. The different positive and negative gains may be effected by varying the gain of the differential amplifier, g_m.

[32]   The gain of the differential amplifier 830 may be varied to accommodate varying degrees of asymmetry by adding, for instance, parallel transistors and switching the parallel transistors in or out of the circuit. This is one manner of altering the gain of the differential amplifier, however, other ways known in the art also may be used. Varying the gain will affect the amount of assymetry. Alternatives include varying IS3 in Fig. 8 in an amount proportional to the square of the current, or varying physical characteristics of transistors 832, 834 in differential amplifier 830 in an amount proportional to the square root of W/L, where W and L are known physical parameters.

[33]   While the invention has been described in detail above with reference to some embodiments, variations within the scope and spirit of the invention will be apparent to those of ordinary skill in the art. Thus, the invention should be considered as limited only by the scope of the appended claims.